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Data receiver with servo controlled delayed clock invention

A Time Ruler is used to periodically discover the Unit Interval (UI) for a ... will clock any far-to-the-right ZEROS in the tapped delay line into SZERO, ...

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Data receiver with servo controlled delayed clock invention

Assuming that the active edge of a bus signal is the rising edge, ... in the data will clock any far-to-the-right ZEROs in the tapped delay line into SZERO, ...

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[PDF] Xilinx XAPP462 Using Digital Clock Managers (DCMs) in Spartan-3 ...

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The minimum delay-line tap resolution, listed as the DCM\_TAP\_MIN ..... only relevant on the active clock edge. For example, in single-data rate (SDR) ...

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[PDF] DS110: "Virtex-II Pro X Platform FPGAs: Advance Product Specification"

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The falling clock edge option uses the BUFGCE\_1. and BUFGMUX\_1 primitives. BUFGCE. If the CE input is active (High) prior to the incoming rising ...

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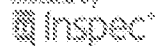
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Wood, Glenn (Agilent Technologies, Inc.(US-DELAWARE)), *UNITED KINGDOM PATENT APPLICATION*, Oct 2005  
patno:GB2412829

...to keep its active edge in the middle...delays the clock is responsive...adjusted clock delay is maintained until active servoing can...to half the unit interval A bank of XOR...the tapped delay line. That number...additional data delay lines, and...the drift in clock phase teeing corrected...discovering Unit Interval using a Time...positioning the active edge of a clock...


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2. [RE-TIMER CIRCUIT FOR DATA RECOVERY WITH FAST RECOVERY FROM A LOW POWER MODE](#)

ABROSI MOV, Igor Anatolievich, *PATENT COOPERATION TREATY APPLICATION*, Feb 2006  
patno:WO06011830

...the re- sampling clock, a tracking pipeline...positioning of the edge of the re-sampling...selector comprises a delay line for generating delayed...outputs from the delay line; a third data...input a reference clock, the delay line...of stages in the delay line, preferably the...inputs to select one tap from the delay line, preferably the...

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Wood, Glenn (Agilent Technologies, Inc.(US-DELAWARE)), *UNITED KINGDOM PATENT APPLICATION*, Oct 2005  
patno:GB2412829  
...location of the active edge of the clock. The result...to a clock delay circuit to...incorporated UNIT INTERVAL DISCOVERY...tapped data delay line, going from...least one unit interval. The various...taps of the delay line for an isolated... Full text available at patent office. For more in-depth searching go to LexisNexis  
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patno:WO06011830  
...the re- sampling clock, a tracking pipeline...positioning of the edge of the re-sampling...selector comprises a delay line for generating delayed...outputs from the delay line; a third data...input a reference clock, the delay line...of stages in the delay line, preferably the...inputs to select one tap from the delay line, preferably the... Full text available at patent office. For more in-depth searching go to LexisNexis  
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...73 7 Sampling Clock Requirements...95 9 8.3.2 Clock Recovery...Figure 3. Jitter is when the sampling clock edge's location changes over time [8, see...  
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Analui, Behnam / Rylyakov, Alexander / Rylov, Sergey / Meghelli, Mounir / Hajimiri, Ali, *article*, Dec 2005  
...lines, i.e., LC networks [3]–[5] or active delay elements [6]. At multigigabit per second data rates, the passive or active delay cells become more sensitive to on-chip...optimizes the phase of the retiming clock. Eye-opening monitor circuits have also...input common mode and . Every positive edge on next\_ref triggers a reference-set...  
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9. [Amplitude monitor for high-speed signals](#)  
Farjad-rad, Ramin, *UNITED STATES PATENT AND TRADEMARK OFFICE PRE-GRANT PUBLICATION*, Jun 2006  
patno: US20060140318  
...next falling edge of sample clock Sclk. Due...an N-stage delay line 700, an embodiment...eight-stage delay line 520 of FIG...tenth of the unit interval (i.e. 0.1...selectable delay line 810, a three-bit...each sample-clock phase, as detailed...  
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...Width 1 byte 1:2(1) N/A 2 byte 1:1 N/A 4 byte 2:1(1) 1:1 8 byte N/A 2:1(1) Notes: 1. Each edge of slower clock must align with falling edge of faster clock. Virtex-II Pro X™ Platform FPGAs: Functional Description R DS110-2 (v1.0) November 17...  
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...reuse the same hardware. Consider the 8-tap filter shown in Figure 19-2. The TDM...with a TDM factor of 2. A 2x-multiplied clock is required to run the filter. On cycle...stored in a register. On cycle 1 of the 2x clock, the user loads the remaining four coefficients...multipliers to achieve the functionality of an 8-tap filter. Thus, TDM is a good way to save...the multipliers can run at n- times the clock speed. The coefficients can be stored...  
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[Assignments](#)Examiner Number: 80488 / [TORRES, JUAN](#)Filing or 371(c) Date: 03/31/2004 [eDan](#)

Group Art Unit: 2611

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Effective Date: 03/31/2004

Class/Subclass: 375/355.000

Application Received: 04/01/2004

Lost Case: NO

Pat. Num./Pub. Num.: /20050220236

Interference Number:

Issue Date: 00/00/0000

Unmatched Petition: NO

Date of Abandonment: 00/00/0000

[L&R Code](#): Secrecy Code: 1

Attorney Docket Number: 10020213-1

Third Level Review: NO

Secrecy Order: NO

Status: 77 /RESPONSE TO EX PARTE QUAYLE ACTION ENTERED  
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Status Date: 01/02/2008

Confirmation Number: 8199

Oral Hearing: NO

Title of Invention: DATA RECEIVER WITH SERVO CONTROLLED DELAYED CLOCK

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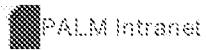
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# Inventor Information for 10/815156

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